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Silicon Genesis Extends Its NANOCLEAVE™ Layer Transfer Technology with New 3DIC Initiatives

August 31, 2023 -- Since introducing its pioneering NANOCLEAVE™ Layer Transfer Technology over twenty-years ago, SiGen has continued to develop and extend from historical applications such as Silicon-on Insulator, Silicon on Quartz and other engineered substrates to new areas. Over the past nine years, SiGen has been quietly developing and working with partners to apply its process and equipment technology to Three Dimensional Integrated Circuit (3DIC) stacking. SiGen is announcing how its technology provides solutions for the most pressing market needs of 3DIC stacking today.

SiGen's NANOCLEAVE™ enables 3DIC without having to restrict process temperature regimes below standard CMOS processing around 1000C° and now enables sequential 3DIC to become a reality.

NANOCLEAVE™ is part of the NANOTEC™ suite of layer transfer process and equipment solutions. This suite of solutions also includes process methods known as POLYMAX™ for making Solar Silicon wafers ranging from 20um to 150um thickness. It also includes proprietary equipment for Room Temperature Controlled Cleaving (rT-CCP) and Plasma Activation (SPA). Please see SiGen's website where the company has continued to market NANOCLEAVE™ and other NANOTEC™ solutions for over twenty years.

Continuing its innovations in layer transfer methods, SiGen has extended its NANOCLEAVE™ process with a new generation of process methods and enabling equipment to perform wafer-scale layer transfer of active IC layers that include devices, metal layers and dielectrics.

Advanced CMOS Image Processors (CIS)

Following its earlier success with 3DIC Mega-pixel CMOS Image Sensors, SiGen is collaborating with partners to apply its NANOCLEAVE™ process to multiple layer CIS products beyond three and four layer stacks. For advanced CIS elements stacked with high-speed signal processing CMOS, the result is a unique combination of multiple layer photo diodes for improved quantum efficiency and light capture, high speed processing,

global shutter capability, high frame rates and long-term operational reliability. This new CIS product will be generations ahead of current CIS processors in the market.

By achieving an active layer of 2um or less, SiGen's layers are two to five times thinner than can be reliably achieved with temporary bond, grind back and etch methods. Also, when compared to interposer stacking using 2.5D packaging methods, the SiGen approach provides an order of magnitude higher signal bandwidth from shorter and denser vertical TSV and metal signal connections, as well as much improved thermal conductivity throughout the atomically bonded stack layers.

Interconnect Network Layers (INL) and Cooling Channels

SiGen has developed and patented a layer transfer approach for an INL that is less than 2um thick. This approach simplifies and reduces the cost associated with Redistribution Layers (RDL). Multiple INL layers and a variety of INL designs can be layer transferred to address the interconnect needs between other INL layers or wafer scale device layers and various heterogeneous devices. In addition, the INL layers increase bandwidth and interconnect density due to reducing TSV aspect ratios to less than 2:1. By integrating cooling channels, this allows for multiple interlayer microfluidic heat dissipation layers that are optimal for cooling 3DIC stacks. Please see the Figure 1 below of cooling channels and dimensions:

Figure 1: Optical, height and 3D images for 10um lines on a transferred layer

High Temperature 1000C^{o} Device Processing

SiGen's NanoCleave™ process also provides alternative sequence steps for layer transfer and CMOS processing. Due to its patented NanoCleave™ process for formation of a cleave plane by implant and/or deposition, and alternative methods for cleave initiation and propagation with a variety of energy sources, a device maker can choose a process and sequence that is optimal for their requirements. This also allows the device maker the option to process devices by pre-imbedding a cleave plane before CMOS processing and allows for normal 1000C^{o} CMOS process temperatures, or by implanting a cleave plane after CMOS device processing has been completed. In either alternative, transferred device layers can be processed without limiting process temperatures to less than 500C^{O} as is the case with other process technologies being offered in the market today.

Patented areas and Competitive Advantage

To summarize, SiGen has extended its NANOCLEAVE™ applications to 3DIC and has been issued a growing number of US and worldwide patents for (1) alternative cleave plane formation and cleave initiation propagation methods, (2) efficient transfer of device layers without damage, (3) imbedded cooling channels, (4) INL layers for higher density TSV and bandwidth, and (5) wafer and mixed die integration layer transfer.

SiGen's business model continues to be the same as it has been over the past twenty years, which is working in close collaboration with customers for technology development and transfer, licensing of its IP and know-how, supported by sale of its proprietary and other third party equipment, and support to maintain the competitive advantage of SiGen licensee customers.

About Silicon Genesis

Silicon Genesis is a leading provider of engineered substrate process technology and equipment for the semiconductor, display, and optoelectronics markets. SiGen's technology is used for production of Silicon-on-Insulator (*SOI*) semiconductor wafers and 3DIC stacks of CMOS device layers for high performance applications. SiGen develops innovative substrates through thin-film and thick-film engineering, enabling new applications and markets for its customers. SiGen's customers and partners include top players from substrate, device and equipment suppliers throughout the world. Founded in 1997, SiGen is headquartered in Fremont, California. For more information, visit www.sigen.com for the complete SiGen NanoTec offerings of layer transfer process, equipment technology and services.